

Code No: D3805, D0602, D7005, D5505, D7709, D5709

R09

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech II - Semester Examinations, March/April 2011

LOW POWER VLSI DESIGN

(COMMON TO DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS,
DIGITAL SYSTEMS & COMPUTER ELECTRONICS, ELECTRONICS &
COMMUNICATION, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI
DESIGN, VLSI SYSTEM DESIGN)

Time: 3hours

Max. Marks: 60

Answer any five questions

All questions carry equal marks

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1. a) What are the various limitations on low voltage and low power design. Explain them.
b) Explain how threshold voltage is adjusted for the CMOS structures in BICMOS devices. [12]
2. a) Explain about the advanced Isolation technique LOCOS.
b) Draw the Retrograde-well CMOS process with neat diagrams. Explain how susceptibility to latch up and punch through is reduced. [12]
3. a) Explain about the prospective technological enhancement for CMOS devices briefly.
b) Explain about SOI CMOS. [12]
4. a) Compare the following two advanced MOSFET models
i) HSPICE level 50 (Philips MOS 9) model.
ii) EKV MOSFET model
b) What are the limitations of the MOSFET characteristics? [12]
5. a) Explain the operation of a high performance complementary coupled BICMOS circuit with neat circuit diagrams.
b) Explain the need for Input protection in BICMOS digital circuit that do not use the input protection circuit. [12]
6. a) Explain about the pipelining theme and high performance and low power theme for latches and flip flops.
b) What are setup time and hold times? Explain the MOCF and setup time and hold time considerations. [12]
7. a) Compare the following BICMOS logic gates CCBICMOS, FSBICMOS, FSCMBL and CIBICMOS circuits with respect to speed, area and power dissipation.
b) What are hot carrier and short channel effects? Explain the impact of short-channel effects on the classical threshold voltage model. [12]
8. Write short notes on any **two**
a) Bipolar SPICE models
b) Lateral BJT on SOI
c) Chemical mechanical polishing. [12]
